output signal by applying the input signal and output signal to gates of transistors which are coupled in a combinational logic circuit.

18. (Amended) A multiplier circuit as claimed in Claim 17 wherein the combinational logic circuit provides current source and drain to an output as up and down current pulses.

REMARKS

It is noted with appreciation that claims 3-4 and 8-9 would be allowable if rewritten in independent form. The claims have not been so rewritten because it is believed that base claims 1 and 6 are allowable for the reasons presented below.

Claims 11-12 and 15-18 were rejected under 35 U.S.C. 112 due to several objections. The claims have been amended to address each of those objections, and reconsideration in view of the amendments is requested.

Claims 1, 5-6 and 10-12 were rejected under 35 U.S.C. 102 as being anticipated by Elder 4,626,796. Claims 2, 8 and 13-14 were rejected under 35 U.S.C. 103 as being unpatentable over Elder. Since claim 8 was indicated to be allowable, it is believed that the reference to claim 8 was a typographical error and that the rejection under 35 U.S.C. 103 had been intended to be applied against claim 7.

The present claims relate to a multiplier such as shown in the embodiment of Fig. 14. At page 12 of the specification, the embodiment of Fig. 14 was compared to the prior art of Fig. 16. The prior art of Figure 16 closely parallels the cited Elder reference. In both Fig. 16 and Elder, an input signal (aclk, 13a) is applied to a phase comparator (194, 13), and an output signal (bclk, 15a) is obtained from a voltage controlled oscillator (192, 15). In each case the output signal is divided down (193, 19) to produce a second input to the comparator (dclk, 13b). As discussed at page 12, by dividing the output of the VCO, a clock dclk of the same frequency as the input clock

aclk is obtained. These two clocks of the same frequency are then compared. Since the input clock is phase locked not to the high frequency output clock, bclk, but rather to the output of the divider, dclk, even when the loop is locked, the edges of aclk and bclk are not aligned. The system of Elder suffers the same result.

By contrast, with the claimed invention, the phase comparator compares the phase of an edge of an input signal with a phase of an edge of the higher rate output signal. Thus, once the loop has acquired lock, the compared rising edges of aclk and bclk are exactly aligned, within the phase offset of the phase comparator. In the embodiment of Fig. 14, phase comparison of the edges of signals of different frequencies is enabled by a windowed phase comparator which receives a window signaled, divided down from the output signal, which identifies the high frequency edges to be compared.

In finding anticipation by Elder, the examiner has referred to signal 15a as an output signal at a rate that is a multiple of input frequency and to signal 13b as an output signal compared to the input signal. However, that interpretation is contrary to the literal wording of the claims. In particular, claim 1 recites "an output signal at a rate that is a multiple of input frequency" which can be compared to signal 15a, and further recites that the phase comparator compares "the phase of an edge of the output signal." The second reference to "the output signal" is to the same signal recited in the first paragraph, that is the output signal which has a rate that is a multiple of the input frequency. In Elder, the signal 13b is not the signal 15a and is not at a rate that is a multiple of the input frequency. It is respectfully submitted that to anticipate the independent claims, the same output signal having a rate that is a multiple of the input frequency must also be applied to the phase comparator, and that is not the case in Elder. Accordingly, the rejection is respectfully traversed and reconsideration is requested.

With respect to claims 2 and 7, the examiner has stated that the use of a window signal that is true during edges of the input signal and output signal would be obvious. However, there is no suggestion in Elder of such a signal which enables comparison of two signals of different frequencies. In fact, Elder teaches away from the claimed invention in that Elder uses the prior

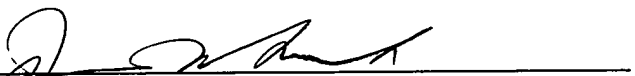
art approach of reducing the frequency of the output signal to obtain a signal to be compared, apparently failing to recognize both the advantage of directly comparing the output signal with the input signal and the ability to perform such a comparison by using a window signal to select one edge of many in the high frequency signal to be compared with an edge of the low frequency signal.

## CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By 

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# MARKED UP VERSION OF AMENDMENTS

Claim Amendments Under 37 C.F.R. § 1.121(c)(1)(ii)

11. (Amended) A method as claimed in Claim 6 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal in combinational circuitry having an output which depends only on the state of an [its] input to the combinational circuitry.

12. (Amended) A method as claimed in Claim 6 wherein the phase comparator produces up and down pulses which, when the phase of the edge of the input signal is aligned with the phase of the edge of the output signal, [are] each have a duration which is a fraction of the input signal and the output signal transition times.

15. (Amended) A multiplier circuit [method] as claimed in Claim 1 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal in combinational circuitry having an output which depends only on the state of an [its] input to the combinational circuitry.

16. (Amended) A multiplier circuit [method] as claimed in Claim 1 wherein the phase comparator produces up and down pulses which, when the phase of the edge of the input signal is aligned with the phase of the edge of the output signal, [are] each have a duration which is a fraction of the input signal and the output signal transition times.

17. (Amended) A multiplier circuit [method] as claimed in Claim 1 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal by applying the input signal and output signal to gates of transistors which are coupled in a combinational logic circuit.

18. (Amended) A multiplier circuit [method] as claimed in Claim 17 wherein the combinational logic circuit provides current source and drain to an output as up and down current pulses.